[0018] FIG. **12** is a schematic plan view illustrating a structure of the connection portion of the groove and the connection groove in the semiconductor device according to one embodiment.

[0019] FIG. **13** is a schematic sectional view illustrating the connection portion in the groove extending direction of the semiconductor device according to one embodiment illustrated in FIG. **12**.

[0020] FIG. **14** is a schematic sectional view illustrating an exemplary structure of a semiconductor device according to another embodiment.

[0021] FIG. **15** is a diagram illustrating a modification example of the structure of the groove in the semiconductor device according to another embodiment.

[0022] FIG. **16** is a schematic plan view illustrating an exemplary arrangement of the groove and the connection groove in the semiconductor device according to one embodiment.

[0023] FIG. **17** is a schematic sectional view illustrating the connection portion in the A-A direction of the semiconductor device according to one embodiment illustrated in FIG. **12**.

DETAILED DESCRIPTION OF EMBODIMENTS

[0024] Embodiments will now be described with reference to the drawings. Note that the same or similar portions are denoted by the same or similar reference numerals in the descriptions of the drawings below. It should be noted, however, that the drawings are schematic only, and that ratios of respective dimensions and the like differ from those in reality. Accordingly, specific dimensions and the like should be determined in consideration of the descriptions below. In addition, some of the dimensional relations and ratios differ in the drawings as a matter of course.

[0025] Moreover, the following embodiments exemplify apparatuses and methods for embodying technical ideas of the invention, by which shapes, structures, and arrangements of components will not be limited to those described below. The embodiments of this invention can be modified in many ways without departing from the scope of claims.

[0026] As illustrated in FIG. **1**, semiconductor device **1** according to one embodiment includes semiconductor substrate **100**, first semiconductor region **10** of a first conductivity type, second semiconductor region **20** of a second conductivity type arranged on first semiconductor region **10**, third semiconductor region **30** of the first conductivity type arranged on second semiconductor region **20**, and fourth semiconductor region **40** of a second conductivity type arranged on third semiconductor region **30**.

[0027] As illustrated in FIG. **1**, grooves **25** are arranged, each groove **25** extending from the top surface of fourth semiconductor region **40** through fourth semiconductor region **40** and third semiconductor region **30** to second semiconductor region **20**. Insulation film **50** is arranged on the inner wall of each of grooves **25**. The inner side walls of groove **25** has control electrodes **60** each arranged on insulation film **50** and facing the side surface of third semiconductor region **30**. The inner bottom wall of groove **25** has bottom electrode **65** arranged on insulation film **50** and spaced from control electrodes **60**. Semiconductor device **1** includes first main electrode **80** electrically connected to first semiconductor region **10** and second main electrode **90** electrically connected to third semiconductor region **30** and fourth semiconductor region **40**. Second main electrode **90** is optionally not electrically connected to third semiconductor region **30**. Bottom electrode **65** is electrically connected to second main electrode **90**.

[0028] The first conductivity type is opposite to the second conductivity type. Namely, if the first conductivity type is the n-type, the second conductivity type is the p-type; if the first conductivity type is the p-type, the second conductivity type is the n-type. An exemplary case will now be described in which the first conductivity type is the p-type and the second conductivity type is the n-type.

[0029] As described above, semiconductor device **1** illustrated in FIG. **1** is a trench gate type IGBT. For easy understanding of explanation, the following description refers to first semiconductor region **10** as p-type collector region **10**, second semiconductor region **20** as n-type drift region **20**, third semiconductor region **30** as p-type base region **30**, and fourth semiconductor region **40** as n-type emitter region **40**. Emitter regions **40** are selectively embedded into part of the top surface of base region **30**. In semiconductor device **1**, the respective semiconductor regions have the following impurity concentrations and thicknesses, for example.

[0030] Emitter region **40** has a thickness of 0.3 μm to 1 μm and an impurity concentration of 1×10^{18} cm^{-3} to 1×10^{20} cm^{-3}. Base region **30** has a thickness of about 4 μm and an impurity concentration of 5×10^{16} cm^{-3} to 1×10^{18} cm^{-3}. Drift region **20** has a thickness of 40 μm or more and 140 μm or less and desirably has a resistivity of 10 Ωcm or more and 150 Ωcm or less. Collector region **10** has thickness of 0.1 μm to 300 μm and an impurity concentration of 1×10^{17} cm^{-3} to 1×10^{19} cm^{-3}.

[0031] In the example illustrated in FIG. **1**, n-type buffer layer **15** is arranged between drift region **20** and collector region **10**.

[0032] The following description refers to Control electrode **60** as gate electrode **60**, first main electrode **80** as collector electrode **80**, and second main electrode **90** as emitter electrode **90**. The surface of base region **30** facing gate electrode **60** defines channel formation region **101**. Namely, the region of insulation film **50** arranged on the side walls of grooves **25** functions as a gate insulation film.

[0033] In semiconductor device **1** illustrated in FIG. **1**, groove **25** has a width W**1** larger than the depth of groove **25**. For example, groove **25** has width W**1** of 3 μm to 20 μm, more preferably 3 μm to 15 μm, still more preferably 6 μm to 15 μm. The groove **25** has a depth of 2 μm to 10 μm, for example, about 5 μm. Width W**1** of groove **25** is preferably larger than gap W**2** of adjacent grooves **25**. For example, gap W**2** between grooves **25** is 2 to 4 μm.

[0034] In the embodiment, width W**1** of groove **25** indicates the width on the extended line of the interface between base region **30** and drift region **20** as illustrated in FIG. **1**. In the embodiment, gap W**2** of the adjacent grooves **25** indicates the gap between grooves **25** on the extended line of the interface between base region **30** and drift region **20**. The width of base region **30** located between grooves **25** and exposed on the surface of semiconductor substrate **100**, i.e., the width of the contact portion of base region **30** and emitter electrode **90** is referred to as "width of a connection region" and is expressed as width W**3** in FIG. **1**. The "width of a connection region" indicates the width orthogonal to the extending direction of groove **25**, which is vertical to the paper in FIG. **1**. Namely, the "width of a connection region" indicates the length parallel to the widthwise direction of groove **25**.